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L1: Entry 1 of 2 File: USPT Feb 25, 2003

US-PAT-NO: 6525557
DOCUMENT-IDENTIFIER: US 6525557 B1

TITLE: Method for watermarking a register-based programmable logic device core

DATE-ISSUED: February 25, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
McManus; James L.	Longmont	CO		
Crabill; Eric J.	San Jose	CA		
Burnham; James L.	Morgan Hill	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Xilinx, Inc.	San Jose	CA			02

APPL-NO: 10/ 053415 [PALM]
DATE FILED: November 2, 2001

INT-CL: [07] H03 K 19/00, H03 K 19/177

US-CL-ISSUED: 326/8; 326/39, 711/163
US-CL-CURRENT: 326/8; 326/39, 711/163

FIELD-OF-SEARCH: 326/8, 326/37, 326/39, 711/163, 711/165, 710/200, 713/200

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5784577	July 1998	Jacobson et al.	710/104
☐	6331784	December 2001	Mason et al.	326/8

OTHER PUBLICATIONS

"The Programmable Logic Data Book", Jan. 29, 1999, (Version 1.5) pp. 6-61-6-68, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124.

ART-UNIT: 2819

PRIMARY-EXAMINER: Tokar; Michael

ASSISTANT-EXAMINER: Cho; James H

ATTY-AGENT-FIRM: Kubodera; John Bever, Hoffman & Harms

ABSTRACT:

A core for a register-based programmable logic device includes a register configured to provide a hidden identifier in response to a secret unlock operation. The identifier is inaccessible during normal operation of the core implementation. The unlock operation is selected to be an action or set of actions that would typically not be performed during normal use of the core implementation. The logic associated with providing the hidden identifier in response to the unlock operation is configured to not interfere with normal operation of the core implementation. Therefore, the presence of this source identification capability is transparent to regular users (and unauthorized copyists) of the core implementation. The availability of the secondary identifier can be limited in duration to minimize the chances of accidental, or even intentional, discovery.

25 Claims, 10 Drawing figures

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End of Result Set

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L1: Entry 2 of 2 File: USPT Sep 18, 2001

US-PAT-NO: 6292020
DOCUMENT-IDENTIFIER: US 6292020 B1

TITLE: Low-skew programmable control routing for a programmable logic device

DATE-ISSUED: September 18, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Crabill; Eric J.	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Xilinx, Inc.	San Jose	CA			02

APPL-NO: 09/ 630034 [PALM]
DATE FILED: August 1, 2000

INT-CL: [07] H03 K 19/177, H01 L 25/00

US-CL-ISSUED: 326/41; 326/41, 326/38, 326/47
US-CL-CURRENT: 326/41; 257/E27.105, 326/38, 326/47

FIELD-OF-SEARCH: 326/38, 326/39, 326/40, 326/41, 326/47

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4642487	February 1987	Carter	
☐	5296759	March 1994	Sutherland et al.	307/465.1
☐	5298805	March 1994	Garverick et al.	307/465
☐	5712579	January 1998	Doung et al.	326/39
☐	6064225	May 2000	Andrews et al.	326/41

OTHER PUBLICATIONS

Xilinx Advance Product Specification, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays", DS025 (v1.0) Mar. 23, 2000, pp. 1-19.

ART-UNIT: 289

PRIMARY-EXAMINER: Tokar; Michael

ASSISTANT-EXAMINER: Tan; Vibol

ATTY-AGENT-FIRM: Behiel; Arthur J.

ABSTRACT:

Described are programmable routing resources capable of distributing low-skew signals along more than one edge of a programmable logic device (PLD). The PLD includes groups of input/output blocks (IOBs) arranged along each edge. A programmable signal-distribution tree can be configured to send a shared, low-skew signal to IOBs along adjacent edges. These signals are conveyed via perpendicular conductive lines that run parallel to the respective edges. Each conductive line can be programmably connected to a source of the shared signal using a respective programmable-interconnect point located near the corner of the PLD defined by the two edges.

17 Claims, 4 Drawing figures

WEST Search History

DATE: Saturday, December 06, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB; PLUR=NO; OP=ADJ			
L9	L8 and L4 and L6	17	L9
L8	fpga or (field programmable gate array$1)	10472	L8
L7	L3 and L4 and L6	6	L7
L6	firmware or nanoinstruction$1 or nano-instruction$1 or nanocode or nano-code or nanoprogram or nano-program or L5	39670	L6
L5	microinstruction$1 or micro-instruction$1 or microcode or micro-code or micro-operation$1 or microoperation$1 or micro-op$1 or microop$1 or micro-program$1 or microprogram$1	12554	L5
L4	macroinstruction$1 or macro-instruction$1 or macrocode or macro-code or macro-operation$1 or macrooperation$1 or macro-op$1 or macroop$1 or macro-program$1 or macroprogram$1 or cisc instruction	1261	L4
L3	reconfigurable.ti,ab.	1624	L3
L2	6081888.uref.	0	L2
L1	crabill.in. and eric.in.	2	L1

END OF SEARCH HISTORY